REMARKS

The Office Action dated February 7, 2005 has been received and carefully noted. The above amendments and the following remarks are submitted as a full and complete response thereto. Claims 3, 6, 9 and 11-15 are pending in this application with claims 2, 4, 5, 7 and 8 cancelled and claims 12-15 added by the present Amendment. In the outstanding Office Action, claims 5 and 6 were objected to and claims 2-9 and 11 were rejected under 35 U.S.C. § 103(a) (two different rejections). No new matter has been added. Accordingly, claims 3, 6, 9 and 11-15 are pending in this application and are submitted for consideration.

Claim Objections

Claims 5 and 6 were objected to because the phrase "an MFS structure or an MFIS structure" in claim 5 and the phrase "an MFMIS structure" in claim 6 are not clear. The cancellation of claim 5 renders this objection moot as to claim 5. The amendment of claim 6 clarifies the phrase "an MFMIS structure". Therefore, Applicants request reconsideration and withdrawal of the objection to claim 6.

35 U.S.C. § 103(a)

Claims 2-8 and 11 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Yamazaki et al. (U.S. Patent No. 5,349,366, "Yamazaki") in view of Black et al. (U.S. Patent No. 6,069,381, "Black"). In making this rejection, the Office Action asserts that the combination of these two references teaches and/or suggests the claimed

invention. The Office Action also asserts that it would be obvious to one of ordinary skill in the art to combine these two references. The cancellation of claims 2, 4, 5, 7 and 8 renders moot the rejection as to these claims. Applicants respectfully traverse the rejection as to claims 3, 6 and 11.

Claim 6, as amended, recites in part:

> ...an MFMIS structure transistor which has a first metal layer, a ferroelectric layer, a second metal layer for gate electrode and an insulator layer provided on a semiconductor layer, a source and drain of said MFMIS structure transistor being connected to said display element and a driving line and said first metal layer being connected to a control line; and
>
> a capacitor connected between said second metal layer and a ground or a write line...

Claim 11, as amended, recites in part:

> ...a MOS transistor, a source and drain of said MOS transistor being connected to said display element and a driving line;
>
> a ferroelectric capacitor connected between a gate of said MOS transistor and a control line; and
>
> a capacitor connected between said gate and a ground or a write line...

In contrast, Yamazaki teaches in Figs. 1(A) and 4(A) a device that includes a display element LC. A transistor Tr2 is connected between the display element LC and a power/voltage supply VLC.

Since the transistor recited in each of independent claims 6 and 11 requires that the source and drain of the transistor be connected to the display element and a driving line, the power supply/voltage supply VLC must be equivalent to the driving line recited in these claims if the transistor Tr2 is the same as the recited transistor.

Fig. 4(A) of Yamazaki illustrates the inherent capacitance of the gate of transistor Tr2 by capacitor C2 shown in dotted lines (phantom lines). Thus, while the capacitance represented by capacitor C2 is real, there is no actual capacitor installed in the system. As shown in Fig. 4(A), the inherent capacitance of the transistor Tr2 of the gate is considered to reside between the gate and the voltage supply line VLC. As discussed above, the voltage supply line VLC must be equivalent to the driving line recited in the claims. Consequently, capacitor C2 is not connected to either a ground or a write line as required by both independent claims 6 and 11. Therefore, capacitor C2 cannot teach and/or suggest a capacitor connected between said second metal layer and a ground or write line as recited in claim 6, or a capacitor connected between said gate and a ground or a write line as recited in claim 11.

The Office Action admits that Yamazaki fails to teach and/or suggest a nonvolatile data holding section capable of holding control data of the control element in a floating state. The Office Action cites Black as correcting this deficiency in Yamazaki.

While Black may teach a ferroelectric memory transistor with a resistively coupled floating gate, Black fails to teach and/or suggest either a capacitor connected between the second metal layer and a ground or a write line as recited in claim 6 or a capacitor connected between the gate and a ground or write line as recited in claim 11.

Consequently, the combination of Yamazaki and Black fails to teach and/or suggest the claimed invention. Regarding claim 6, the combination of these two references fails to teach and/or suggest a capacitor connected between the second metal layer and a ground or a write line. Regarding claim 11, the combination of these two references fails to disclose and/or suggest a capacitor connected between the gate

and a ground or a write line. Claim 3 depends from claim 6. Accordingly, Applicants respectfully request reconsideration and withdrawal of the rejection of claims 3, 6 and 11 under 35 U.S.C. § 103(a).

Claim 9 was rejected under 35 U.S.C. § 103(a) as being unpatentable over Yamazaki in view of Black and further in view of Nakamura (U.S. Patent No. 6,563,480). In making this rejection, the Office Action asserts that the combination of these three references teaches and/or suggests the claimed invention. The Office Action also asserts that it would be obvious to one of ordinary skill in the art to combine these three references. Applicants respectfully request reconsideration of this rejection.

As an initial matter, Nakamura is neither cited for, nor does Nakamura teach, either a capacitor connected between the second metal layer and a ground or write line as recited in claim 6 or a capacitor connected between the gate and a ground or a write line as recited in claim 11.

Applicants also assert that it would not be obvious to combine Nakamura with Black and Yamazaki since the use of an organic EL element for the display element uses a different voltage drive circuit than a liquid crystal display element. Specifically, the organic EL element is driven by an electric current.

Consequently, Applicants assert that it would not be obvious to combine these three references. In the event that these three references were combined, the combination of these three references fails to teach and/or suggest the claimed invention. Specifically, the combination of these three references fails to teach and/or suggest a capacitor connected between the second metal layer and a ground or a write

line. Therefore, Applicants request reconsideration and withdrawal of the rejection of claim 9 under 35 U.S.C. § 103(a).

New Claims

New claims 12-15 have been added to claim additional embodiments of Applicants' invention.

New claims 12 and 13 depend from claim 11 and are allowable for at least the same reasons discussed above for claim 11.

Regarding new claims 14 and 15, Applicants have carefully reviewed the cited prior art and could find no disclosure and/or suggestion that the nonvolatile data holding section could be formed from an element using a magnetoresistance effect or a single electron memory.

Consequently, the combination of the cited prior art fails to teach and/or suggest the claimed invention. Specifically, the combination of the cited prior art fails to teach and/or suggest that the nonvolatile data holding section is constituted by an element utilizing a magnetoresistance effect or a single electron memory. Therefore, Applicants respectfully request consideration and allowance of new claims 14 and 15.

Conclusion

Applicants' remarks have overcome the objection and rejections set forth in the Office Action dated February 7, 2005. Specifically, Applicants' cancellation of claim 5 and amendments to claim 6 have overcome the objection of these claims. Applicants remarks have distinguished claims 3, 6 and 11 from the combination of Yamazaki and

Black and thus overcome the rejection of these claims under 35 U.S.C. § 103(a). Applicants' remarks have distinguished claim 9 from the combination of Yamazaki, Black and Nakamura and thus overcome the rejection of this claim under 35 U.S.C. § 103(a). Applicants' remarks have distinguished new claims 12-15 from the cited prior art. Accordingly, claims 3, 6, 9 and 11-15 are in condition for allowance. Therefore, Applicants request reconsideration and allowance of claims 3, 6, 9 and 11-15.

Applicants submit that the application is now in condition for allowance. If the Examiner believes the application is not in condition for allowance, Applicants respectfully request that the Examiner contact the undersigned attorney by telephone if it is believed that such contact will expedite the prosecution of the application.

In the event that this paper is not considered to be timely filed, Applicants respectfully petition for an appropriate extension of time.

The Commissioner is authorized to charge payment for any additional fees which may be required with respect to this paper to our Deposit Account No. 01-2300, making reference to attorney docket number 107400-00021.

Respectfully submitted,
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